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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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06/29/2000

Takaaki Nagai

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22428

7590

02/13/2003

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EXAMINER

BROCK II, PAUL E

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/606,159

Applicant(s)

NAGAI ET AL.

Examiner

Paul E Brock II

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 December 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-24 and 26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 21-24 and 26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 June 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 09/124,851.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 21 – 24 and 26 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not clear where in the originally filed specification where support for “said plurality of word lines being perpendicular to... said plurality of first polysilicon strips;” “said first metal wiring layer... portions of said first metal wiring layer having a width wider than a diameter of said contact holes;” “said first metal wiring layer does not make contact with said plurality of field insulating films;” and “said first metal wiring layer is formed with a raised portion only above ones of said plurality of contact holes formed above said source regions, and is formed in an island shape above ones of said plurality of contact-holes formed above said drain regions;” “ can be found.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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4. Claims 21 – 24 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. It is not clear how a word line can be perpendicular to the polysilicon strips. In the step of forming the word lines, the polysilicon strips are etched into floating gates. Therefore, after the step of defining the word lines, there are no longer any polysilicon strips. How can something be perpendicular to that which does not exist? Therefore, the relationships defined with regard to “said plurality of word lines being perpendicular to... said plurality of first polysilicon strips,” are indefinite. ✓

6. It is not clear in the step of “said first metal wiring layer... portions of said first metal wiring layer having a width wider than a diameter of said contact holes,” if the “said first metal wiring layer” is already patterned into “a common source line... and a plurality of bit studs.” Does the “portions of said first metal wiring layer having a width wider than a diameter of said contact holes” define a portion of the “common source line” or the “plurality of bit studs”? Does the “portions of said first metal wiring layer having a width wider than a diameter of said contact holes” define the first metal wiring layer before it is patterned? Any portion of a first metal wiring layer is defined as either a common source line or a bit line in the forming step. Is there another section of the first wiring layer besides the common source line or bit lines that are being defined?

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7. Further “said first metal wiring layer extends in parallel with said plurality of field insulating films” is unclear due to a similar problem as above. Is the first metal wiring that is being referred to the common source line or bit studs? Is there another section of the first wiring layer besides the common source line or bit lines that are being defined?

8. Similarly, “said first metal wiring layer is formed with a raised portion only above ones of said plurality of contact holes formed above said source regions, and is formed in an island shape above ones of said plurality of contact-holes formed above said drain regions,” is unclear for the same reasons. Is the claim language referring to either of the common source line or bit studs? Is this claim language defining other features that are not included by the common source line or bit studs?

9. As is disclosed in the specification: “forming a first metal wiring layer which is patterned so as to form both a common source line extending in parallel with the word lines and connecting source regions to one another, and an extended bit line connecting the drain region to a bit line;” and claimed “forming a first metal wiring layer which is patterned so as to form both a common source line extending in parallel with said plurality of word lines and connecting source regions to one another and a plurality of bit studs extending to said drain regions, said first metal wiring layer being formed above a surface of said first interlayer insulating layer;” it should be noted that once the first metal wiring layer is patterned, it is no longer the “first metal wiring layer,” but is now “a common source line” and “a bit line.” To further define a first metal wiring layer, after the patterning step, is confusing and misleading.

Claim Rejections - 35 USC § 103

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claims 21, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya et al. (USPAT 5838615, Kamiya) in view of Nishihara (JPPAT 08204159) and Kim (USPAT 5741719).

Kamiya discloses a method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors in figures 1 – 7.

With regard to claim 21, Kamiya discloses in figures 1 and 4 forming a plurality of field insulating films (101) in parallel with one another on a semiconductor substrate (100). Kamiya discloses in figure 1 forming a first gate insulating film (103 and 106a) in each of active regions. Kamiya then discloses in figure 1 forming a plurality of first polysilicon strips (107a) in parallel with one another. Kamiya further discloses in figure 1 that forming a second gate insulating film (106) and a second polysilicon layer (107) all over the product resulting from the above steps.

As best the examiner can ascertain Kamiya discloses in figure 1 patterning the second polysilicon layer, the second gate insulating film, and the first polysilicon strips to thereby form a plurality of control gates (107) and floating gates (107a), the plurality of control gates serving as a plurality of word lines, the plurality of word lines being perpendicular to the plurality of field insulating films and the plurality of first polysilicon strips. Kamiya discloses in figure 1 forming drain (109a) and source (109) regions. Kamiya also discloses in figure 1 forming a first

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interlayer insulating layer (111) over the product resulting from the above steps. Kamiya discloses in figure 1 forming contact-holes through the first interlayer insulating layer above both the drain and source regions in the plurality of memory cell transistors. Kamiya does not teach that the contact-holes are formed only above the drain and source regions in the plurality of memory cell transistors. Nishihara teaches contact-holes that are formed only above drain and source regions in a plurality of memory cell transistors. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the contact holes of Nishihara in the method of Kamiya in order to form working memory cell transistors. Kamiya discloses in figure 4 forming a first metal wiring layer which is patterned so as to form both a common source line (114 and 115) extending in parallel with one another and connecting source regions to one another and a plurality of bit studs (113 and 115) extending to the drain regions. Kamiya discloses in figures 6 and 7 forming a second metal wiring layer (118a) that is patterned so as to form a bit line and connecting the drain regions with each another. Kamiya does not teach forming a second interlayer insulating layer all over the product resulting from the steps before forming the second metal wiring layer. Kamiya further does not teach the bit line having a top portion and a bottom portion. Kim teaches in figure 6 and column 3, lines 10 – 15 forming a second interlayer insulating layer (78) all over a product before forming a second metal wiring layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the interlayer insulating film of Kim in the process of forming a second metal wiring layer of Kamiya and Nishihara in order to form a more complicated wiring scheme as is well known in the art. Kim further teaches in figure 10c forming a second metal wiring layer which is patterned so as to form a bit line (80) extending perpendicularly to a plurality of word

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lines (50) and connecting the drain regions with each other, the bit lines having a top portion (73) and a bottom portion (69) with the top portion being wider than the bottom portion, wherein the bottom portion of the bit line is connected to the top portion of the plurality of bit studs and the bottom portion of the plurality of bit studs is connected to the drain regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bit line with a top and bottom portion of Kim in the method of Kamiya in order to form a bit line in a long rod shape in the direction of the Y-axis and is shared by cell transistor's drains adjacent in the direction of the Y-axis as stated by Kim in column 11, lines 23 – 25. As best the examiner can ascertain Kamiya, Nishihara, and Kim teach the first metal wiring layer fills therewith all of the contact-holes formed above the drain and source regions, portions of the first metal wiring layer having a width wider than a diameter of the contact holes. As best the examiner can ascertain Kamiya, Nishihara, and Kim the first metal wiring layer extends in parallel with the plurality of field insulating films above the plurality of field insulating films with respect to a distance from the semiconductor substrate such that the first metal wiring layer does not make contact with the plurality of field insulating films. As best the examiner can ascertain Kamiya, Nishihara, and Kim the first metal wiring layer is formed with a raised portion only above ones of the plurality of contact-holes formed above the source regions, and is formed in an island shape above ones of the plurality of contact-holes formed above the drain regions.

With regard to claim 22, Kamiya discloses in column 4, lines 46 – 51 that the second gate insulating film has a three-layer structure of oxide/nitride/oxide films.

12. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya, Nishihara and Kim. as applied to claim 21 above, and further in view of Yonemoto.

Kamiya does disclose in column 5, lines 62 – 63 that the second wiring layers are composed of aluminum. Kamiya, Nishihara and Kim do not disclose forming the first wiring layer of aluminum. Yonemoto does disclose forming a first wiring layer composed of aluminum in column 5, lines 8 – 11. It would have been obvious to use the aluminum wiring of Yonemoto in the process of Kamiya, Nishihara and Kim in order to form signal lines to connect to the source region as stated by Yonemoto in column 5, lines 8 – 11.

13. Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya in view of Nishihara, Kim, and Cacharelis et al. (USPAT 5550072, Cacharelis).

With regard to claim 24, Kamiya discloses in figures 1 and 4 forming a plurality of field insulating films (101) in parallel with one another on a semiconductor substrate (100). Kamiya discloses in figure 1 forming a first gate insulating film (103 and 106a) in each of active regions. Kamiya then discloses in figure 1 forming a plurality of first polysilicon strips (107a) in parallel with one another. Kamiya further discloses in figure 1 that forming a second gate insulating film (106) and a second polysilicon layer (107) all over the product resulting from the above steps. As best the examiner can ascertain Kamiya discloses in figure 1 patterning the second polysilicon layer, the second gate insulating film, and the first polysilicon strips to thereby form a plurality of control gates (107) and floating gates (107a), the plurality of control gates serving as a plurality of word lines, the plurality of word lines being perpendicular to the plurality of field insulating films and the plurality of first polysilicon strips. Kamiya also discloses in figure 1

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forming drain (109a) and source (109) regions. Kamiya also discloses in figure 1 forming a first interlayer insulating layer (111) over the product resulting from the above steps. Kamiya discloses in figure 1 forming contact-holes through the first interlayer insulating layer above both the drain and source regions in the plurality of memory cell transistors. Kamiya does not teach that the contact-holes are formed only above the drain and source regions in the plurality of memory cell transistors. Nishihara teaches contact-holes that are formed only above drain and source regions in a plurality of memory cell transistors. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the contact holes of Nishihara in the method of Kamiya in order to form working memory cell transistors. Kamiya discloses in figure 4 forming a first metal wiring layer which is patterned so as to form both a common bit line (114 and 115) extending in parallel with one another and connecting bit regions to one another and a plurality of source studs (113 and 115) extending to the source regions, the plurality of source studs have a top portion (connected to the source line) and a bottom portion (connected to the source region) with the top portion of the plurality of source studs being wider than the bottom portion of the plurality of source studs, the first metal wiring layer being formed above a surface of the first interlayer insulating layer. Kamiya does not disclose forming a second metal wiring layer that is patterned so as to form a common source line connecting the source regions to one another. Kamiya does not disclose forming a second interlayer insulating layer all over the product resulting from the steps before forming the second metal wiring layer. Kim teaches in figure 8g and column 6, lines 51 – 55 forming a first metal wiring layer which is patterned so as to form both a bit line 71 extending almost in parallel with field insulating films and connecting drain regions to one another, and an extended common source pad (73)

connecting the source region to a later mentioned common source line. While Kim describes the feature 71 as a source line, it is accepted in the art that a process used to make features of a source line can be interchanged with a process used to make a drain line. Kim teaches in figure 6 and column 3, lines 10 – 15 forming an interlayer insulating layer (78) all over a product. Kim teaches in figure 8g forming a second metal wiring layer (80) which is patterned so as to form a common source line connecting the source regions with each another, the common source line having a top portion and a bottom portion with the top portion of the common source line being wider than the bottom portion of the common source line, wherein the bottom portion of the common source line is connected to a top portion (73) of a plurality of source studs and a bottom portion of the plurality of source studs (69) is connected to a source region. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the wiring processes and interlayer insulating film of Kim in the fabrication of an EEPROM semiconductor device of Kamiya in order to overcome the integration limitations caused by standard photolithography methods as stated by Kim in column 1, lines 52 – 60. As best the examiner can ascertain Kamiya, Nishihara, and Kim teach the first metal wiring layer fills therewith all of the contact-holes formed above the drain and source regions, portions of the first metal wiring layer having a width wider than a diameter of the contact holes. As best the examiner can ascertain Kamiya, Nishihara, and Kim the first metal wiring layer extends in parallel with the plurality of field insulating films above the plurality of field insulating films with respect to a distance from the semiconductor substrate such that the first metal wiring layer does not make contact with the plurality of field insulating films. As best the examiner can ascertain Kamiya, Nishihara, and Kim the first metal wiring layer is formed with a raised portion only above ones of the plurality

of contact-holes formed above the source regions, and is formed in an island shape above ones of the plurality of contact-holes formed above the drain regions.

Kamiya, Nishihara and Kim do not disclose forming backing wiring layers. Cacharelis teaches in figure 20a forming backing wiring layers (490 and 500) connecting to a control gate at a certain interval and are constituted of a second metal wiring layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the backing wires of Cacharelis in the method of Kamiya, Nishihara and Kim in order to form a word lines as stated in column 5, lines 50 – 53.

Response to Arguments

14. Applicant's arguments filed December 4, 2002 have been fully considered but they are not persuasive.

15. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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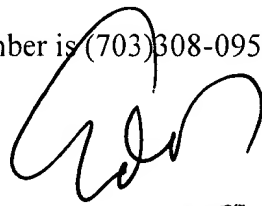

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
February 10, 2003



EDDIE LEE
SUPERVISORY PATENT EXAMINER
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